REMARKS

Claims 1, 10, 16 and 27 have been canceled, and claims 32-34 have been added. Claims 2-9, 11-15, 17-20, and 23-25 have been amended. Upon entry of the amendment, claims 2-9, 11-15, 17-26 and 28-34 will be pending. Reconsideration is respectfully requested in light of the following remarks.

Provisional Double Patenting Rejection:

The Examiner provisionally rejected claims 1-31 under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over claims 1-36 of copending Application No. 10/027,353. Applicant acknowledges this provisional rejection and will address the rejection should the rejection become non-provisional.

Section 103(a) Rejection:

The Final Action rejected claims 1, 4-6, 12, 16, 20, 25, 27, and 28 under 35 U.S.C. § 103(a) as being unpatentable over Fossum et al. (U.S. Patent 4,888,679) (hereinafter "Fossum") in view of Sollars (U.S. Patent 6,216,218), claims 2, 15, 17 and 18 as being unpatentable over Fossum in view of Sollars, and further in view of McClure (U.S. Patent 5,590,307) (hereinafter, "McClure"), claims 3 and 19 as being unpatentable over Fossum in view of Sollars, and further in view of Faraboschi et al. (U.S. Patent 6,122,708) (hereinafter "Faraboschi"), claims 7, 8, 21 and 22 as being unpatentable over Fossum in view of Sollars, and further in view of Handy ("The Cache Memory Book: The Authoritative Reference on Cache Design," Academic Press, 1993, page 57), claims 9-11, 23 and 24 as being unpatentable over Fossum in view of Sollars, and further in view of Microsoft ("Microsoft Computer Dictionary," Microsoft Press, 2002, page 391: parity), claims 13, 14 and 26 as being unpatentable over Fossum in view of Sollars, and further in view of Morton (U.S. Patent 6,088,783) (hereinafter, "Morton"), and claims 29 and 30 as being unpatentable over Fossum in view of Sollars and Morton, and further in

view of Microsoft. Applicant traverses these rejections and submits that the pending claims are distinguishable over the cited art as set forth in greater detail below.

Regarding claim 32, the cited art fails to teach or suggest a storage array including a plurality of mass storage devices, and an array controller configured to perform block operations on data stored to the storage array, wherein the array controller includes a cache accumulator memory configured as a cache of a memory and a functional unit configured to perform a block operation on one or more block operands to generate a block result, wherein in response to an instruction using an address in the memory to identify a first block operand, the cache accumulator memory is configured to output the first block operand to the functional unit and to accumulate an intermediate result of a block accumulation operation performed on the first block operand, wherein the intermediate result is both a result of and an operand of the block accumulation operation.

In rejecting claim 1 in the Final Action, the Examiner argues that while Fossum does not explicitly state that a cache memory is configured to accumulate an intermediate result that is both a result and an operand, such behavior is "exactly the intended purpose of a cache memory," in that caches "store data that is needed currently, or soon to be needed... [and] thus intermediate results will certainly be accumulated and stored in the cache memory." Applicant strongly disagrees with the Examiner's interpretation of Fossum in view of the specific language of Applicant's claim 32. That a cache may be configured to store data that is produced by one operation and utilized by another operation is not in any way suggestive of a cache accumulator memory that is configured to accumulate an intermediate result of a block accumulation operation, where the intermediate result is both a result of and an operand of the block accumulation operation. The Examiner seems to suggest that storing data in a cache is equivalent to an accumulation operation. However, Applicant has recited a specific relationship between the result of a block accumulation operation and an operand of the block accumulation operation that is not in any way inherent in the data storage operation of a cache as a cache is conventionally understood or disclosed by Fossum.

Moreover, the cited art neither teaches or suggests any aspect of a storage array including a plurality of mass storage devices or an array controller configured to perform block operations on data stored to the storage array, as recited in claim 32. In particular, neither Fossum nor Sollars, the references used to reject claim 1 in the Final Action, teaches or suggests any aspect of these features. Both Fossum and Sollars are directed to various aspects of scalar and vector processor designs, and make no mention of block accumulation operations performed in the context of a storage array system.

For at least these reasons, Applicant submits that claim 32 is distinguishable over the cited art, as are claims 33 and 34 having similar limitations to claim 32.

Applicant notes that a similar argument applies to previously presented claim 28, which has not been amended herein. According to the Final Action, claim 28 is rejected as unpatentable over Fossum in view of Sollars for the reasons given in rejecting claim 1. *However, Applicant notes that claim 28 recites numerous features that are not recited in claim 1 and are not suggested by Fossum or Sollars, either individually or in combination.* Thus, the Examiner's rejection based merely on the same reasons as given for claim 1 is clearly improper. Moreover, neither Fossum nor Sollars teaches or suggests a data processing system including a host computer system coupled to a storage array via an interconnect, where the system includes a parity calculation system configured to perform parity operations on data, and where the parity calculation system includes a cache accumulator memory similar to that recited in claim 32. As argued above, Fossum and Sollars are collectively silent with respect to storage systems, and neither reference teaches or suggests the specific arrangement of elements configured as recited in claim 28. Moreover, neither reference discloses any aspect of performing parity operations on data stored to a storage array.

Therefore, for at least the foregoing reasons, Applicant submits that claim 28 is distinguishable over the cited art.

Applicant notes that numerous ones of the dependent claims recite additional distinctions over the cited art. However, as the independent claims have been shown to be distinguishable, further discussion of the dependent claims is unnecessary at this time.

CONCLUSION

Applicant submits the application is in condition for allowance, and notice to that effect is respectfully requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-05200/RCK.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

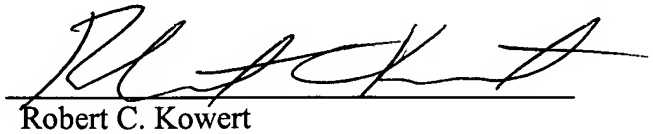
☐ Petition for Extension of Time

☐ Notice of Change of Address

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



Robert C. Kowert
Reg. No. 39,255
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8850

Date: May 26, 2005